

Soft-Switching PWM Full-Bridge Converters

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- Backgrounds
- PWM Strategies for Soft-Switching Full-Bridge Converters
- ZVS PWM Full-Bridge Converters
- ZVZCS PWM Full-Bridge Converters
- Conclusion





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Buck-Derived Converters

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Among the buck-derived converters, the **full-bridge** converter can output **maximum power**, given that the power switches have the **same voltage and current ratings**.



Applications of Full-Bridge Converters



The full-bridge converter have widely used in medium-to-high power dc-dc conversions:

Switching-mode rectifier for telecommunications, power system, etc.;

electroplating power supply;

dc-dc converters for electrical-powered vehicles.

dc-dc converters for aircraft, ship and satellites.









Objectives of This Presentation







Reveal the relationship among the existing modulation strategies

Reveal the relationship among the existing topologies

Propose other modulation strategies and topologies





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Basic Operating Principle of Full-Bridge Converter





PWM Strategies for Full-Bridge Converter





A Family of PWM Strategies for FB Converter

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According to the <u>turn-off sequence</u> of the <u>diagonal switches</u>, the family of PWM strategies can be divided into two categories:

- 1. the diagonal switches turn off simultaneously;
- 2. the turn-off instances of the diagonal switches are staggered. One turns off before the other.



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 $v_A > v_B$



 Q_1 和 Q_4 是 零电压关断 v_{AB} V_{in} Q_1 Q_2 $\frac{D_2}{B}$ () A V_{in} V_{in} Q_4 Q_3 L_{lk} $D_3\overline{C}_3$ $D_4 C_4$ $D_{R1} C$ L_f R_{Ld} i_p i_p . + +0 V_o *V_{rect}* D $t_0 t_1 t_2 t_3$ t_4 ₽ D_{R2}

 $v_A > v_B$ both the two rectifier diode conduct







 Q_1 和 Q_4 是 零电压关断 v_{AB} V_{in} Q_2 Q_1 A V_{in} V_{in} $Q_1 和 Q_4 是$ Q_4 L_{lk} D_3C_3 $D_4 C_4$ 硬开通 $Q_2 和 Q_3 是$ D_{R1} C R_{Ld} 硬开通 i_p i_p V_o **V**_{rect} $t_0 t_1 t_2 t_3$ t_4 ₽ D_{R2}

☺ If the diagonal switches turn off simultaneously, the power switches CAN NOT realize soft-switching.





If the <u>turn-off instances</u> of the <u>diagonal</u> <u>switches is staggered</u>, the switching transition will be improved.

1. the switches turning off firstly constitute the LEADING LEG;

2. the switches turning off lately constitute the LAGGING LEG.





When the leading switch turns off, the current flowing out/into point A is the reflected output filter inductor current, a nearly constant current source.

- the leading leg CAN ONLY realize zero-voltage-switching (ZVS), and CANNOT realize zero-currentswitching (ZCS);
- \odot the leading leg is easier to realize ZVS.











The Lagging Leg Realizes ZVS



- the lagging switches should have capacitors in parallel with them, so that they can realize ZVS;
- ONLY the leakage inductor provides energy for achieving ZVS for the lagging leg, so the lagging leg is difficult to realize ZVS than the leading leg.



The Lagging Leg Realizes ZCS



- the lagging switches can realize ZCS if zero state operating in current reset mode.;
- The lagging switches should have No capacitor in parallel with them.
- At zero state, when the primary current i_p decays to zero, it should keep at zero.





The realization of soft-switching for the power switches **DOES NOT** require any auxiliary power switch, it utilizes **appropriate switching mechanism** of the four power switches.





ZVS Type: The Switching of Lagging Switches



In order to ensure ZVS for the lagging switches, the turn-off time instant of the lagging switches should be delayed to $T_s/2$, i.e., the conducting time of the lagging switches should be $T_s/2$.



ZVS Type: The Switching of Leading Switches



Since i_p flowing through the anti-paralleled diode of Q_3 at zero state, the turnon instant can be at any time, so the conduction time of the leading switches can be three kinds.



 v_{AB}

 Q_1

 Q_3

 Q_4

 Q_2

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 $2\bar{T}_{on}^6$

 $T_s/2$

 T_s

0

ZVS Type: PWM Strategies



ZVZCS Type: The Switching of Leading Switches

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In order to ensure zero-voltage turn-on of the leading switches, the turn-on time instant should be moved forward and let the conducting time to be $T_s/2$.

ZVZCS Type: The Switching of Lagging Switches

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^(*) In order to ensure zero-current turn-off of the lagging switches, the turn-off time instant should be delayed to the time when i_p is reset or even to let the conducting time to be $T_s/2$.

ZVZCS Type: PWM Strategies

 v_{AB} Q_{1} Q_{3} Q_{4} Q_{2} Q_{4} Q_{2} U_{O} T_{on} $T_{s}/2$ T_{s}

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Basic ZVS PWM Full-Bridge Converter

V_{in} O_4 L_{lk} D_{R1} C R_{Ld} l_p Vrect D_{R2}

Advantages

- The junction capacitors of the power switches and the leakage inductor of the transformer are **fully** used to achieve ZVS for the power switches.
- No auxiliary power switches and element is required. This leads to simple topology.
- It operates with constant frequency, leading to easy optimization of the transformer and input and output filter.
- Various commercial controller IC are available, leading to simple implementation of control circuit.

Characteristics

- The leading leg can realize ZVS in a wide load range because both the energy stored in the filter inductor and leakage inductor are utilized.
- The lagging leg is relatively difficult to realize ZVS since only the energy stored in the leakage inductor is used.
- The leakage inductor or external resonant inductor results in duty cycle loss, thus the primary-to-secondary turns ratio of the transformer should be reduced, which leading to high voltage stress of the rectifier diodes and primary current stress..

Increase Load-Range of ZVS for Lagging Switches

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Increase Load-Range of ZVS for Lagging Switches

The auxiliary inductor current increases with the load current

Increase Load-Range of ZVS for Lagging Switches

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The auxiliary inductor current is adaptive with the load current, i.e., it is reduced as the load current increases.

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Block Voltage Source for Resetting Primary Current

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Implementation of Block Voltage Source

Blocking Reverse Flowing Path of *i*^{*p*} **at Zero State**

<u>Possible places to block the reverse</u> <u>flowing path of i_p </u>

- AC/AO segment; X
- AB segment;
- **BC/BO** segment.

Blocking Reverse Flowing Path of *i*^{*n*} **at Zero State**

AB segment to block the reverse flowing path of i_p

Blocking Reverse Flowing Path of *i*^{*p*} **at Zero State**

AB segment to block the reverse flowing path of i_p

Blocking Reverse Flowing Path of *i*^{*p*} **at Zero State**

<u>BC/BO segment to block the reverse flowing path of i_p </u>

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- A family of PWM strategies are proposed for full-bridge converter, which can be divided into two categories: one is that the diagonal switches turn off simultaneously, and the other is that the diagonal switches turn off at different time instance. The form one cannot achieve soft-switching for the power switches, and the latter one provides the possibility of achieve soft-switching, thus the concept of LEADING LEG and LAGGING LEG is introduced.
- The leading leg CAN ONLY and is EASY to realize ZVS, and the lagging leg can realize ZVS or ZCS, thus the soft-switching PWM full-bridge converter can be categorized into two kinds: One is ZVS type, for which both the leading leg and lagging leg realize ZVS; and the other one is ZVZCS type, for which the leading leg realize ZVS, and the lagging leg realize ZCS. The suitable PWM strategies for ZVS type and ZVZCS type full-bridge converter are pointed out.

- For ZVS PWM full-bridge converter, the leading leg is easier to realize ZVS than the lagging leg. Some auxiliary circuits to help the lagging leg to realize ZVS are presented.
- For ZVZCS PWM full-bridge converter, the method of resetting the primary current at zero state are proposed, and the relationship of the several existing topologies are revealed. Furthermore, a new topology is proposed.

Thanks for your attention !

Questions? / Answer!